Table of Contents: Volume 4 (1992)

Number 1

Special Issue: Application Specific Array Processors
Guest Editors: Jose Fortes and Wojtek Przytula

Introduction ..... *Jose Fortes and Wojtek Przytula* 5

A Method for Implementation of One-Dimensional Systolic Algorithms with Data Contraflow Using Pipelined Functional Units *Miguel Valero-García, Juan J. Navarro, José M. Llabería, Mateo Valero and Tomás Lang* 7

Calculus of Space-Optimal Mappings of Systolic Algorithms on Processor Arrays ..... *Philippe Clauss, Catherine Mongenet, and Guy-René Perrin* 27

A Four Megabit Dynamic Systolic Associative Memory Chip ..... *G.J. Lipovski* 37

VLSI Algorithms and Architectures for Complex Householder Transformation with Applications to Array Processing ..... *C.F.T. Tang, K.J.R. Liu, S.F. Hsieh, and K. Yao* 53

Bit-Level Systolic Algorithms for Real-Time Symmetric and Hermitian Eigenvalue Problems ..... *Jean-Marc Delosme* 69

Numbers 2/3

Special Issue: 1990 Workshop on VLSI Signal Processing
Guest Editor: Kung Yao

Introduction ..... *Kung Yao* 95

Quasi-Linear Allocation Functions for Efficient Array Design ..... *Xiaoxiong Zhong and Sanjay Rajopadhye* 97

Parallel Implementation of Neural Networks ..... *K. Wojtek Przytula, Viktor K. Prasanna, and Wei-Ming Lin* 111

MSSM—A Design Aid for Multi-Stage Systolic Mapping ..... *Yin-Tsung Hwang and Yu Hen Hu* 125

VLSI Parallel Architecture for Kalman Filter: An Algorithm Specific Approach *Magdy A. Bayoumi, Padma Rao, and Bassem Alhalabi* 147

A Radix-8 Wafer Scale FFT Processor ..... *Earl E. Swartzlander, Jr., Vijay K. Jain, and Hiroomi Hikawa* 165

High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation ..... *H.R. Srinivas and Keshab K. Pahri* 177

Power Dissipation of VLSI Array Processing Systems ..... *Paul M. Chau and Scott R. Powell* 199

DDFSGEN: A Silicon Compiler for Direct Digital Frequency Synthesizers ... *Linda Kwai-Lin Lau, Rajeev Jain, Henry Samueli, Henry T. Nicholas, III, and Etan G. Cohen* 213

Regular Papers

Systolic Inner Product Arrays with Automatic Word Rounding ..... *M. Yan and J.V. McCanny* 227

Initializing RAM-Based Logarithmic Processors ..... *M.G. Arnold, T.A. Bailey, J.R. Cowles, and J.J. Cupal* 243

Number 4

Nonlinear Transformations for High Level Regular Array ASIC Synthesis ..... *Michaël F.X.B. van Swaaij, Francky V.M. Catthoor and Hugo J. De Man* 259
High Performance VLSI Architecture for Wave Digital Filtering ..... *Rajinder Jit Singh and J.V. McCanny* 269
Systemic Generation of Linear Allocation Functions in Systolic Array Design ..... *Xiaoxiong Zhong, Sanjay Rajopadhye and Ivan Wong* 279
Fault-Tolerance in FFT Arrays: Time Redundancy Approaches ..... *A. Antola, R. Negrini, M.G. Sami and N. Scarabottolo* 295
A Resource-Efficient Reconfiguration Algorithm of VLSI 2-D Processor Arrays ..... *Jung H. Kim and Phill K. Rhee* 317
Error Detection in Arrays via Dependency Graphs ... *Edwin Hsing-Mean Sha and Kenneth Steiglitz* 331
Multidimensional Fourier Transforms by Systolic Architectures ..... *T.D. Roziner and M.G. Karpovsky* 343
High-Speed Digital Filtering: Structures and Finite Wordlength Effects . *K.S. Arun and D.R. Wagner* 355
A Study of VLSI Symmetric FIR Filter Structures ..... *Zhi-Jian (Alex) Mou* 371